Power Management IC Series for Mobile Phones

High-efficiency Power Management IC

BH6172GU

Pb Free ROHM Electronic Components

RoHS Directive Compliance

● Descriptions

BH6172GU incorporates 1 DCDC+ 5 Linear LDO regulators.

It is integrated in a small 2.6mm×2.6mm size package, with 16 steps adjustable Vo's for every channel,

low voltage output (0.8V~) to support almost any kind of mobile application now available.

● Features

   1) 1ch 500mA, high efficiency Step-down Converter. (16 steps adjustable VO by I^2C)

   2) 5-channel CMOS-type LDOs. (16 steps adjustable VO by I^2C, 150mA × 3, 300mA × 2)

   3) Power ON/OFF control enabled by I2C interface or external pin

   4) I^2C compatible Interface. (Device address is "1001111")

   5) Wafer Level CSP package(2.6mm × 2.6mm) for space-constrained applications

   6) Discharge resistance selectable for power-down sequence ramp speed control

   7) Over-current protection in all LDO regulators

   8) Over-current protection in Step-down Converter

   9) Over-voltage protection in Step-down Converter

   10) Thermal shutdown protection

● Applications

Mobile phones, Portable game systems, Portable mp3 players, Portable DVD players, Portable TV, Portable GPS,
PDA, Portable electronic dictionaries, etc.

● Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Maximum Supply Voltage (VBAT)	VBATMAX	6.0	V
Maximum Supply Voltage (PBAT)	VPBATMAX	6.0	V
Maximum Supply Voltage (VUSB)	VUSBMAX	6.0	V
Maximum Supply Voltage (DVDD)	DVDDMAX	4.5	V
Maximum Input Voltage 1 (LX, FB, OUT1, OUT2, OUT3, OUT4, OUT5, EN_LD1, EN_LD2, EN_LD3, EN_LD4)	VINMAX1	VBAT + 0.3	V
Maximum Input Voltage 2 (NRST, CLK, DATA)	VINMAX2	DVDD + 0.3	V
Power Dissipation	Pd	900[1]	mW
Operating Temperature Range	Topr	-35 ～ +85	℃
Storage Temperature Range	Tstg	-55 ～ +125	℃

* This is an allowable loss of the ROHM evaluation glass epoxy board(60mm × 60mm × 16mm).

   To use at temperature higher than 25℃ , derate 9.0mW per 1℃.

**   Must not exceed Pd or ASO.

● Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Range	Unit
VBAT Voltage	VBAT	*2 2.20 ～ 5.50	V
PBAT Voltage	VPBAT	*2 2.20 ～ 5.50	V
VUSB Voltage	VUSB	*2*3 2.20 ～ 5.50	V
DVDD Voltage	VDVDD	*4 1.70 ～ 4.20	V

*2 Whenever the VBAT or PBAT or VUSB voltage is under the LDO, SWREG output voltage,
or else under certain levels, the LDO and SWREG output is not guaranteed to meet its published specifications.
*3 VUSB Power Supply can be externally connected to the VBAT, PBAT Power Supply when necessary.
*4 The DVDD Voltage must be under the Battery Voltage VBAT, PBAT at any times.

● Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Circuit Current						
VBAT Circuit Current 1 (OFF)	IQVB1	-	0.4	1	μA	LDO1～5=OFF SWREG1=OFF NRST=L DVDD=0V
VUSB Circuit Current 1 (OFF)	IQUSB1	-	0	1	μA	
VBAT Circuit Current 2 (OFF)	IQVB2	-	0.4	1	μA	LDO1～5=OFF SWREG1=OFF NRST=L DVDD=0V VUSB=VBAT external connection
VBAT Circuit Current 3 (STANDBY)	IQVB3	-	0.7	1.4	μA	LDO1～5=OFF SWREG1=OFF NRST=H DVDD=2.6V
VUSB Circuit Current 2 (STANDBY)	IQUSB2	-	0	1	μA	
VBAT Circuit Current 4 (STANDBY)	IQVB4	-	0.7	1.4	μA	LDO1～5=OFF SWREG1=OFF NRST=H DVDD=2.6V VUSB=VBAT external connection
VBAT Circuit Current 5 (Active)	IQVB5	-	170	300	μA	LDO1～5=ON(no load, initial voltage) SWREG1=ON(no load, initial voltage) NRST=H DVDD=2.6V
VUSB Circuit Current 3 (Active)	IQUSB3	-	35	70	μA	
VBAT Circuit Current 6 (Active)	IQVB6	-	200	350	μA	LDO1～5=ON(no load, initial voltage) SWREG1=ON(no load, initial voltage) NRST=H DVDD=2.6V VUSB=VBAT external connection

◎This product is not especially designed to be protected from radioactivity.

● Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V, DVDD=2.6V)

Logic pin character							
NRST (CMOS input)	Input "H" level	VIH1	$0.7\times$ DVDD	-	DVDD+ 0.3	V	Pin voltage: DVDD
	Input "L" level	VIL1	-0.3	-	$0.3\times$ DVDD	V	Pin voltage: 0 V
	Input leak current	IIC1	0	0.3	1	μA	
EN_LD1, EN_LD2, EN_LD3, EN_LD4 (NMOS input)	Input "H" level	VIH2	1.44	-	-	V	
	Input "L" level	VIL2	-	-	0.4	V	
	Input leak current	IIC2	-1	0	1	μA	
Digital characteristics (Digital pins: CLK and DATA)							
Input "H" level		VIH3	$0.8\times$ DVDD	-	DVDD + 0.3	V	
Input "L" level		VIL3	-0.3	-	$0.2\times$ DVDD	V	
Input leak current		IIC3	-1	0	1	μA	Pin voltage: DVDD
DATA output "L" level voltage		VOL	-	-	0.4	V	IOL=6mA

● Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SWREG						
Output Voltage	VOSW	0.94	1.00	1.06	V	initial value Io=100mA
Output current	IO$_{SW}$	-	-	500	mA	Vo=1.00V
Efficiency	η SW	-	90	-	%	Io=100mA, Vo=2.40V, VBAT=3.2V
Oscillating Frequency	f$_{OSC}$	-	1.7	-	MHz	Vo=1.00V
Output Inductance	L$_{SWREG}$	1.5	2.2	-	μH	Ta= -30～75°C
Short circuit current	I$_{SHTSW}$	-	500	-	mA	Ta= -30～75°C
Output Capacitance	C$_{SWREG}$	3.3	4.7	-	μF	Ta= -30～75°C with SWREG's DC bias

● Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LDO1						
Output Voltage	VOM1	0.970	1.000	1.030	V	initial value Io=1mA@VBAT=4.5V Io=150mA@VBAT=3.4V
Output current	VOM1C	-	-	150	mA	Vo=1.0V
Dropout Voltage	VOM1DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	$\triangle$VIM1	-	2	-	mV	VBAT=3.4～4.5V, Io=50mA Vo=1.0V
Load Stability	$\triangle$VLM1	-	20	-	mV	Io=50μA～150mA, VBAT=3.6V Vo=1.0V
Ripple rejection ratio	RRM1	-	60	-	dB	V_R=-20dBV f_R=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Short circuit current	I_{SHTM3}	-	180	-	mA	Vo=0V
Output Capacitor	C_{OUT1}	-	1.0	-	μF	Ta= -30～75°C with LDO's DC bias
LDO2						
Output Voltage	VOM2	2.522	2.600	2.678	V	initial value Io=1mA@VBAT=4.5V Io=150mA@VBAT=3.4V
Output current	VOM2C	-	-	150	mA	Vo=2.6V
Dropout Voltage	VOM2DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	$\triangle$VIM2	-	2	-	mV	VBAT=3.4～4.5V, Io=50mA Vo=2.6V
Load Stability	$\triangle$VLM2	-	20	-	mV	Io=50μA～150mA, VBAT=3.6V Vo=2.6V
Ripple rejection ratio	RRM2	-	60	-	dB	V_R=-20dBV f_R=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Short circuit current	I_{SHTM3}	-	180	-	mA	Vo=0V
Output Capacitor	C_{OUT2}	-	1.0	-	μF	Ta= -30～75°C with LDO's DC bias
LDO3						
Output Voltage	VOM3	2.716	2.800	2.884	V	initial value Io=1mA@VBAT=4.5V Io=150mA@VBAT=3.4V
Output current	VOM3C	-	-	300	mA	Vo=2.8V
Dropout Voltage	VOM3DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	$\triangle$VIM3	-	2	-	mV	VBAT=3.4～4.5V, Io=50mA Vo=2.8V
Load Stability	$\triangle$VLM3	-	20	-	mV	Io=50μA～300mA, VBAT=3.6V Vo=2.8V
Ripple rejection ratio	RRM3	-	60	-	dB	V_R=-20dBV f_R=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Short circuit current	I_{SHTM3}	-	180	-	mA	Vo=0V
Output Capacitor	C_{OUT3}	-	1.0	-	μF	Ta= -30～75°C with LDO's DC bias

● Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LDO4						
Output Voltage	VOM4	1.746	1.800	1.854	V	initial value Io=1mA@VBAT=4.5V Io=300mA@VBAT=3.4V
Output current	VOM4C	-	-	300	mA	Vo=1.8V
Dropout Voltage	VOM4DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	$\triangle$VIM4	-	2	-	mV	VBAT=3.4～4.5V, Io=50mA Vo=1.8V
Load Stability	$\triangle$VLM4	-	30	-	mV	Io=50μA～300mA, VBAT=3.6V Vo=1.8V
Ripple rejection ratio	RRM4	-	60	-	dB	V_R=-20dBV f_R=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Short circuit current	I_{SHTM4}	-	340	-	mA	Vo=0V
Output Capacitor	C_{OUT4}	-	1.0	-	μF	Ta= -30～75°C with LDO's DC bias
LDO5						
Output Voltage	VOM5	3.201	3.300	3.399	V	initial value Io=1mA@VUSB=5.5V Io=150mA@VUSB=4.4V
Output current	VOM5C	-	-	150	mA	Vo=3.3V
Dropout Voltage	VOM5DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	$\triangle$VIM5	-	2	-	mV	VUSB=4.4～5.5V, Io=50mA Vo=3.3V
Load Stability	$\triangle$VLM5	-	20	-	mV	Io=50μA～150mA, VUSB=5.5V Vo=3.3V
Ripple rejection ratio	RRM5	-	60	-	dB	V_R=-20dBV f_R=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Short circuit current	I_{SHTM5}	-	180	-	mA	Vo=0V
Output Capacitor	C_{OUT5}	-	1.0	-	μF	Ta= -30～75°C with LDO's DC bias

● SWREG & LDOs Output Voltage table

	Usage example	Power Supply	Initial Output Voltage	Load max	Adjustable range
SWREG	CORE	VBAT/PBAT	1.00V	500mA	0.80-2.40V
LDO1	CORE	VBAT	1.00V	150mA	1.00-3.30V
LDO2	I/O1	VBAT	2.60V	150mA	1.00-3.30V
LDO3	MEMORY	VBAT	2.80V	300mA	1.20-3.30V
LDO4	I/O2	VBAT	1.80V	300mA	1.20-3.30V
LDO5	USB	VBAT/VUSB	3.30V	150mA	1.20-3.30V

		SWREG	LDO1	LDO2	LDO3	LDO4	LDO5
Programmable Output Voltages		0.80V	1.00V	1.00V	1.20V	1.20V	1.20V
		0.85V	1.10V	1.10V	1.30V	1.30V	1.30V
		0.90V	1.20V	1.20V	1.40V	1.40V	1.40V
		0.95V	1.30V	1.30V	1.50V	1.50V	1.50V
		1.00V	1.40V	1.40V	1.60V	1.60V	1.60V
		1.05V	1.50V	1.50V	1.70V	1.70V	1.70V
		1.10V	1.60V	1.60V	1.80V	1.80V	1.80V
		1.15V	1.70V	1.70V	1.85V	1.85V	1.85V
		1.20V	1.80V	1.80V	1.90V	1.90V	1.90V
		1.365V	1.85V	1.85V	2.00V	2.00V	2.00V
		1.40V	2.60V	2.60V	2.60V	2.60V	2.60V
		1.50V	2.70V	2.70V	2.70V	2.70V	2.70V
		1.65V	2.80V	2.80V	2.80V	2.80V	2.80V
		1.80V	2.85V	2.85V	2.85V	2.85V	2.85V
		1.85V	3.00V	3.00V	3.00V	3.00V	3.00V
		2.40V	3.30V	3.30V	3.30V	3.30V	3.30V

● Block diagram, Ball matrix

Fig.1 Block diagram

Fig.2 Ball matrix

● Pin description

Ball No.	PIN Name	Function
B4	DATA	Data input/output for I²C
C4	CLK	CLK input for I²C
E1	VBAT1	Power Supply 1
E4	VBAT2	Power Supply 2
A5	PBAT	Power Supply for SWREG
A4	LX	Inductor Connect pin for SWREG
A3	PGND	Ground for SWREG
B5	FB	Voltage Feed back pin for SWREG
D4	NRST	RESET Input Pin (Low Active)
D5	OUT1	LDO1 Output
D1	OUT2	LDO2 Output
E5	OUT3	LDO3 Output
E3	OUT4	LDO4 Output
A1	OUT5	LDO5 Output
B1	REFC	Reference Voltage Output
C2	EN_LD1	LDO1 Enable Pin
D2	EN_LD2	LDO2 Enable Pin
D3	EN_LD3	LDO3 Enable Pin
C3	EN_LD4	LDO4 Enable Pin
A2	VUSB	*1 USBVBUS Power Supply
C5	DVDD	Digital Power Supply
C1	GND	Analog Ground
B3	TEST	TEST PIN (Always keep OPEN at normal use)
E2	TEST2	TEST PIN (Always keep OPEN at normal use)

*TEST, TEST2 pin is used during our company shipment test.
 Please keep TEST pin and TEST2 pin "OPEN" at all times.
*1 VUSB Power Supply can be externally connected to the VBAT Power Supply when necessary.

● I²C Bus INTERFACE

The I²C compatible synchronous serial interface provides access to programmable functions and register on the device.
This protocol uses a two-wire interface for bi-directional communications between the LSI's connected to the bus.
The two interface lines are the Serial Data Line(DATA), and the Serial Clock Line(CLK). These lines should be connected to
the power supply DVDD by a pull-up resistor, and remain high even when the bus is idle.

1.Start and Stop Conditions
  When CLK is high, pulling DATA low produces a start condition and pulling DATA high produces a stop condition.
  Every instruction is started when a start condition occurs and terminated when a stop condition occurs.
  During read, a stop condition causes the read to terminate and the chip enters the standby state.
  During write, a stop condition causes the fetching of write data to terminate, after which writing starts automatically.
  Upon the completion of writing, the chip enters the standby state. Two or more start conditions cannot be entered
  consecutively.
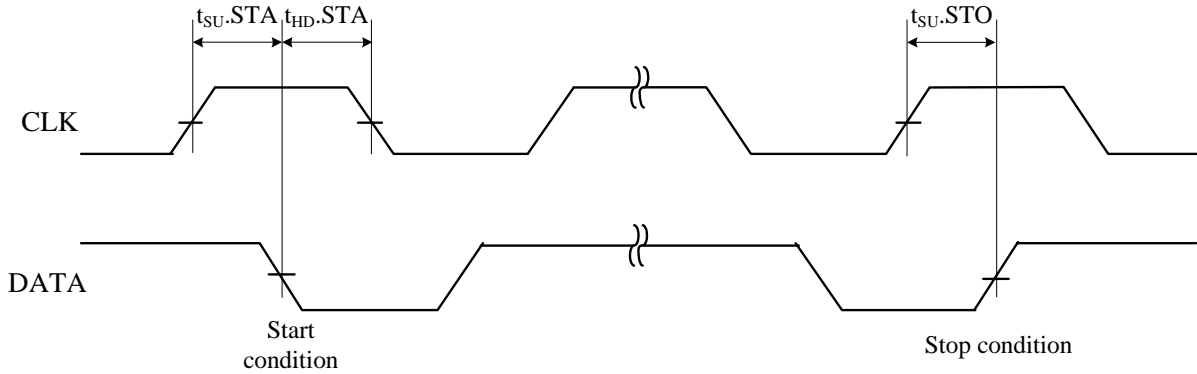
Fig.3   I²C Start, Stop condition

2.Data transmission
  Data on the DATA input can be modified while CLK is low. When CLK is high, modifying the DATA input means a start or
stop condition.
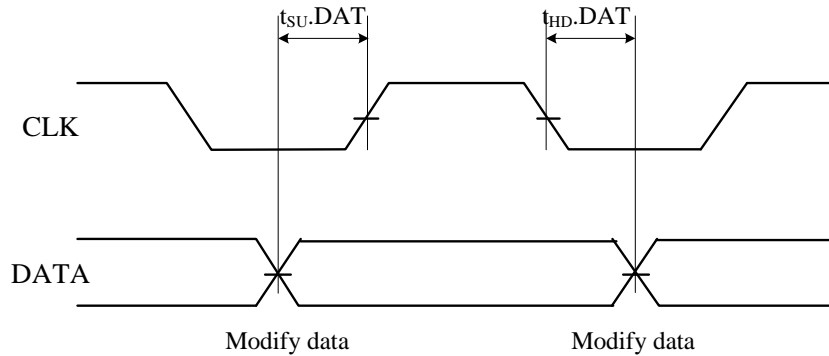
Fig.4   I²C Data Transmission Timing

  All other acknowledge, write, and read timings all conform to the I²C standard.

3.Device addressing

  The device address for this device is "1001111".
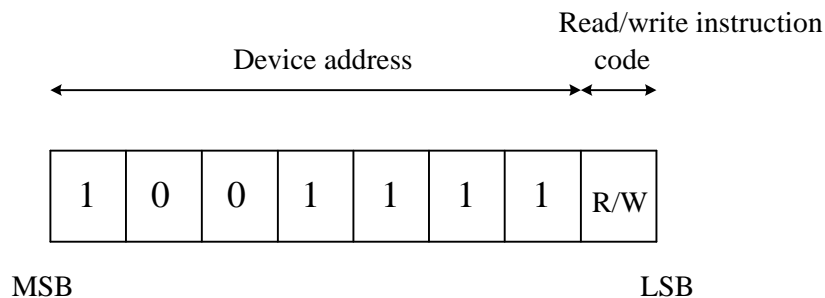
Fig.5   I²C device address

● I²C Bus　AC specification

Characteristics	Symbol	Min	Max	Unit
CLK clock frequency	fCLK	0	400	kHz
CLK clock "low" time	tLOW	1.3	-	μs
CLK clock "high" time	tHIGH	0.6	-	μs
Bus free time	tBUF	1.3	-	μs
Start condition hold time	tHD.STA	0.6	-	μs
Start condition setup time	tSU.STA	0.6	-	μs
Data input hold time	tHD.DAT	0	-	ns
Data input setup time	tSU.DAT	100	-	ns
Stop condition setup time	tSU.STO	0.6	-	μs
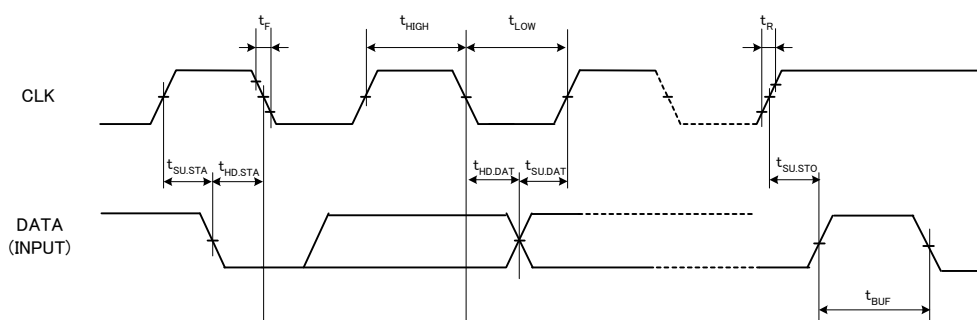
Fig.6　Bus timing 1
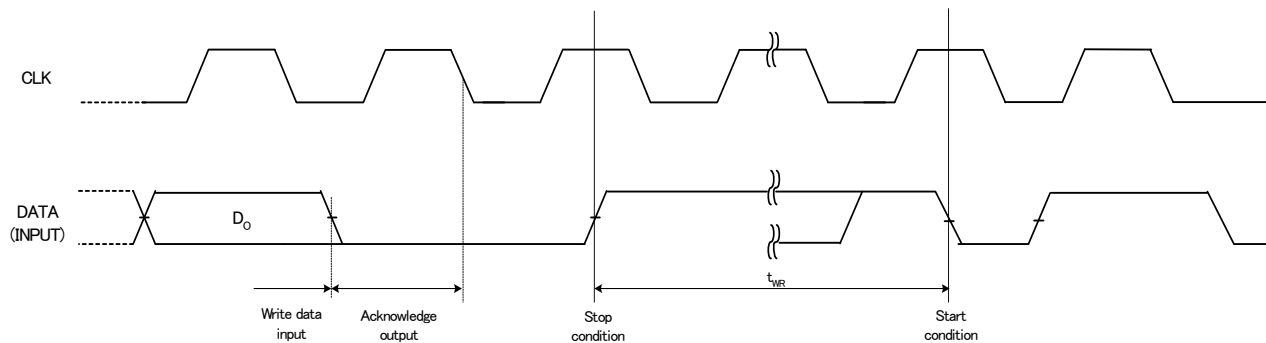
Fig.7　Bus timing 2

● I²C Register information

○REGCNT(SWREGON, LDO*ON)

Control each SWREG, LDO.

0	ON
1	OFF

○SWADJ(SWREGADJ[3:0])

Change SWREG output voltage by 16 steps.

"0000"	0.80V
～	～
"1111"	2.40V

○LDOADJ*(LDO*ADJ[3:0])

Change LDO1～5 output voltage by 16 steps.

"0000"	1.00V(LDO1, 2), 1.20V(LDO3, 4, 5)
～	～
"1111"	3.30V

○PDSEL(SWPDSEL, LDO*PDSEL)

Change the discharge resistance of SWREG, LDO.

0	1kΩ
1	10kΩ

○PDCNT(SWPD, LDO*PD)

Enable/disable the discharge resistance of SWREG, LDO.

0	Discharge disable
1	Discharge enable

○EN_SEL(ENLD*_EN)

Select either an enable pin or I²C register for LDO1～4 ON/OFF control.

0	External enable pin selected
1	I²C register selected

● Reference data(ICC)

ICC(OFF) VUSB=5.0V

ICC(OFF) VBAT=VUSB short

ICC(STBY) VBAT=VUSB short

ICC(ACTIVE) VBAT=VUSB short

● Reference data(SWREG)

SWREG Line Regulation VO=1.0V

SWREG Load Regulation VO=1.0V

SWREG Efficiency vs Io (Vo=1.365V)   VBAT=3.6V
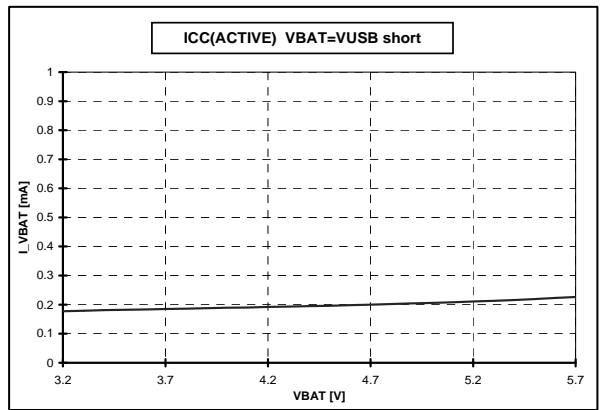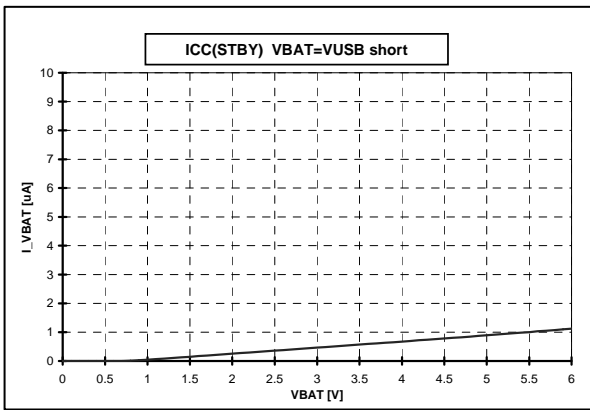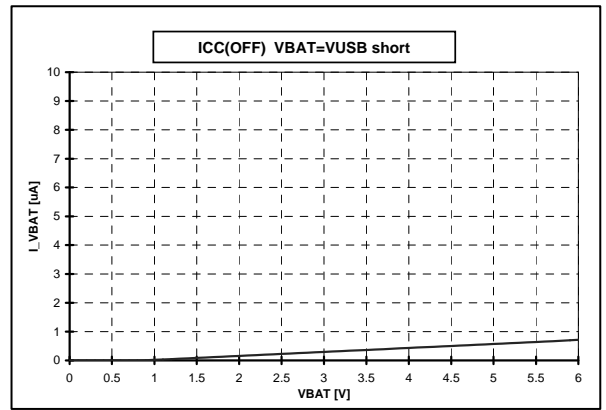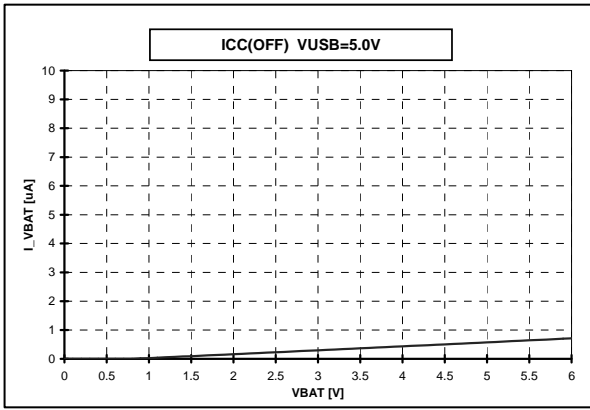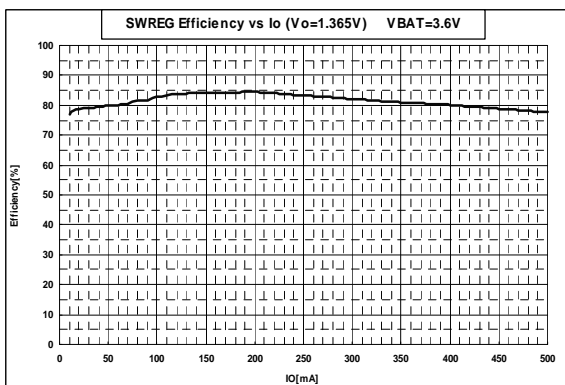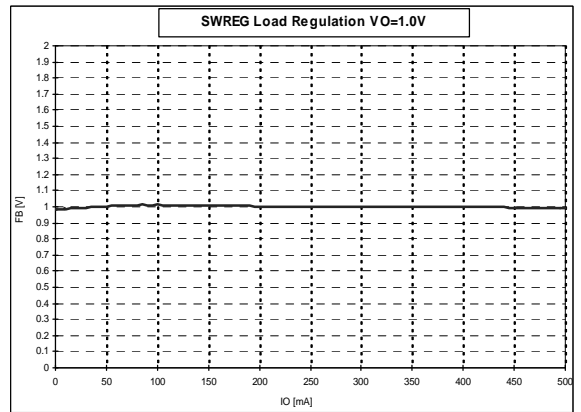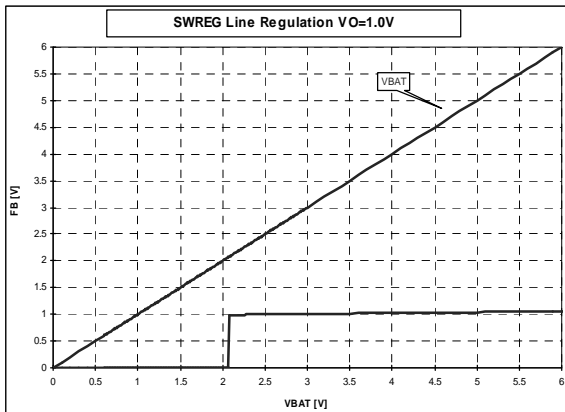
● Reference data(Output stability)

LDO1 Load Regulation 1.20V

LDO2 Load Regulation 2.60V

LDO3 Load Regulation 3.0V

LDO4 Load Regulation 1.80V

LDO5 Load Regulation 3.30V
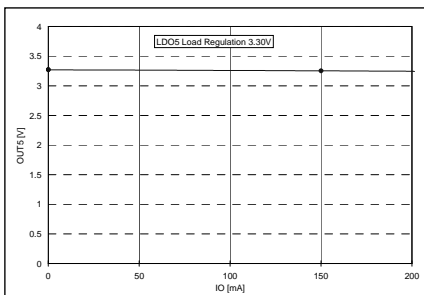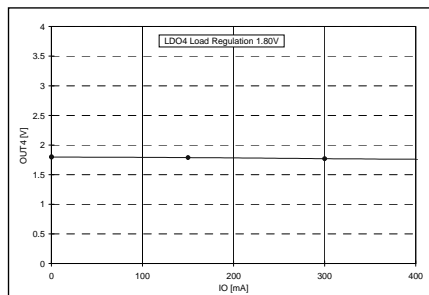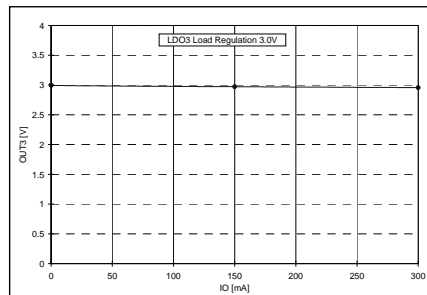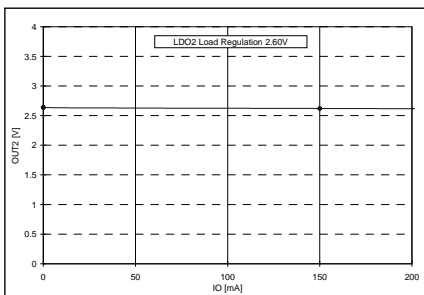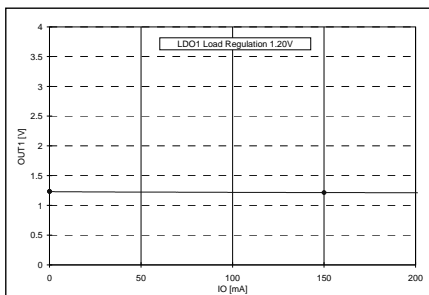
● Reference data(Input stability)

LDO1 Line Regulation 1.20V

LDO2 Line Regulation 2.60V

LDO3 Line Regulation 3.0V

LDO4 Line Regulation 1.80V

LDO5 Line Regulation 3.30V
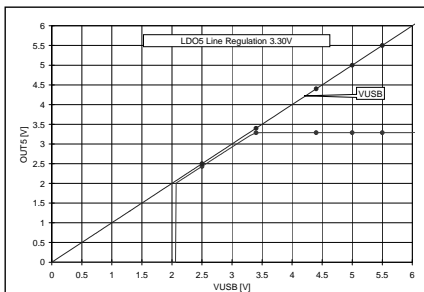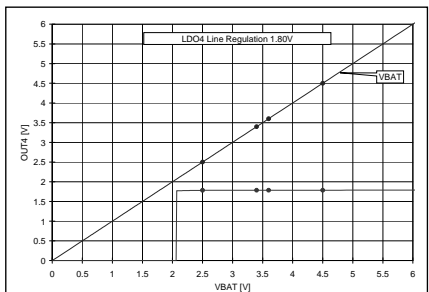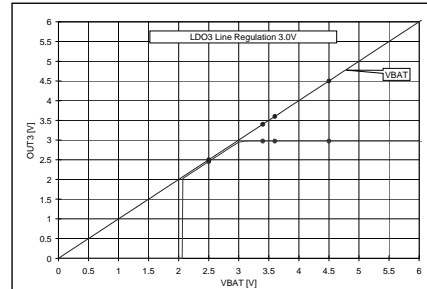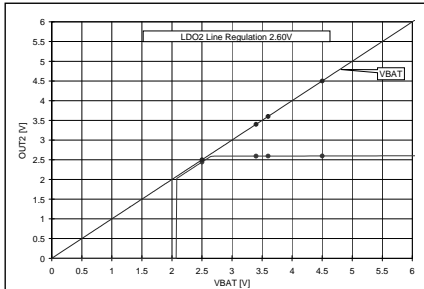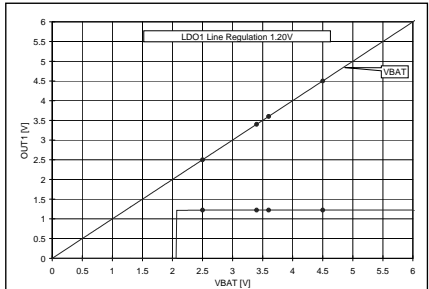
● Reference data(Load transient response)

LDO1

LDO2

LDO3

LDO4

LDO5
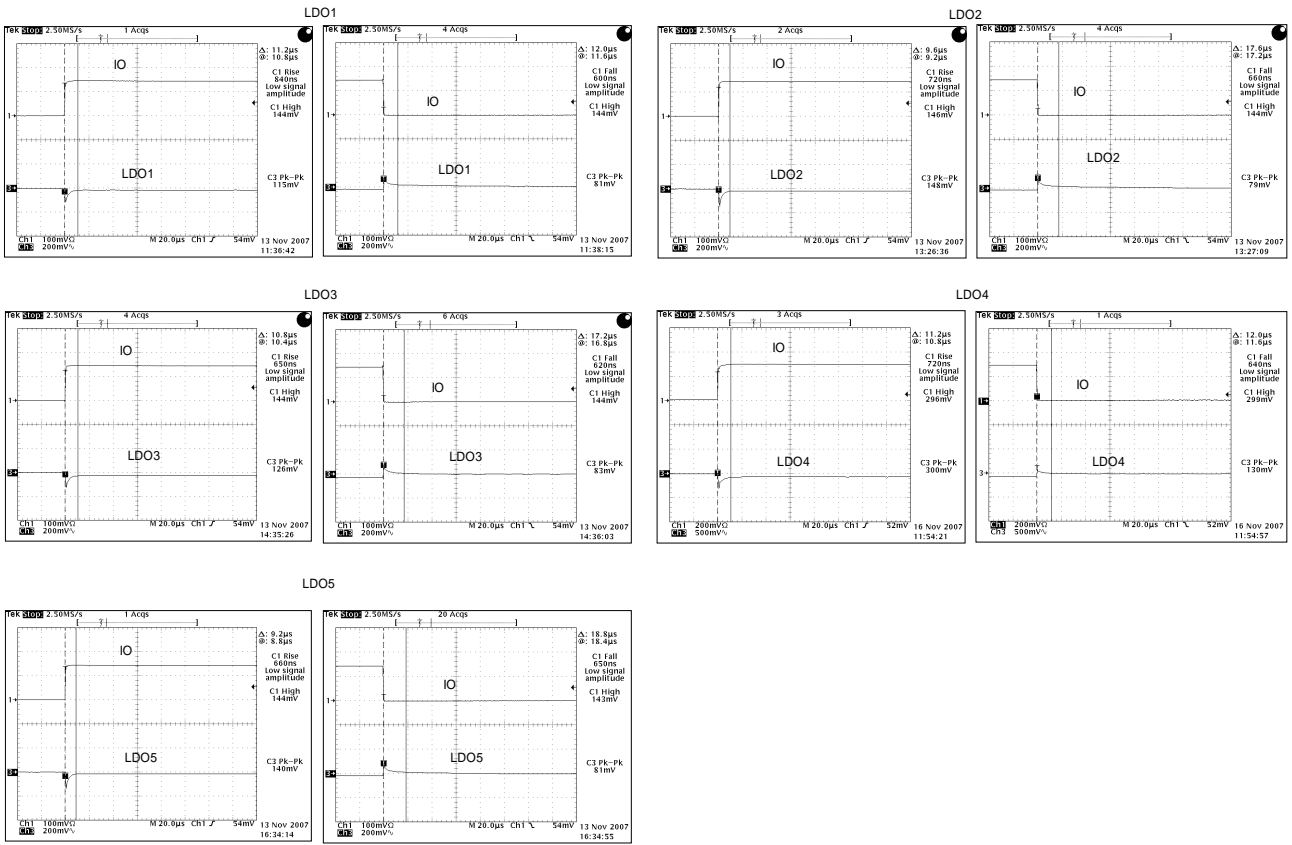
● Reference data(Rise time)

LDO1

LDO2

LDO3

LDO4
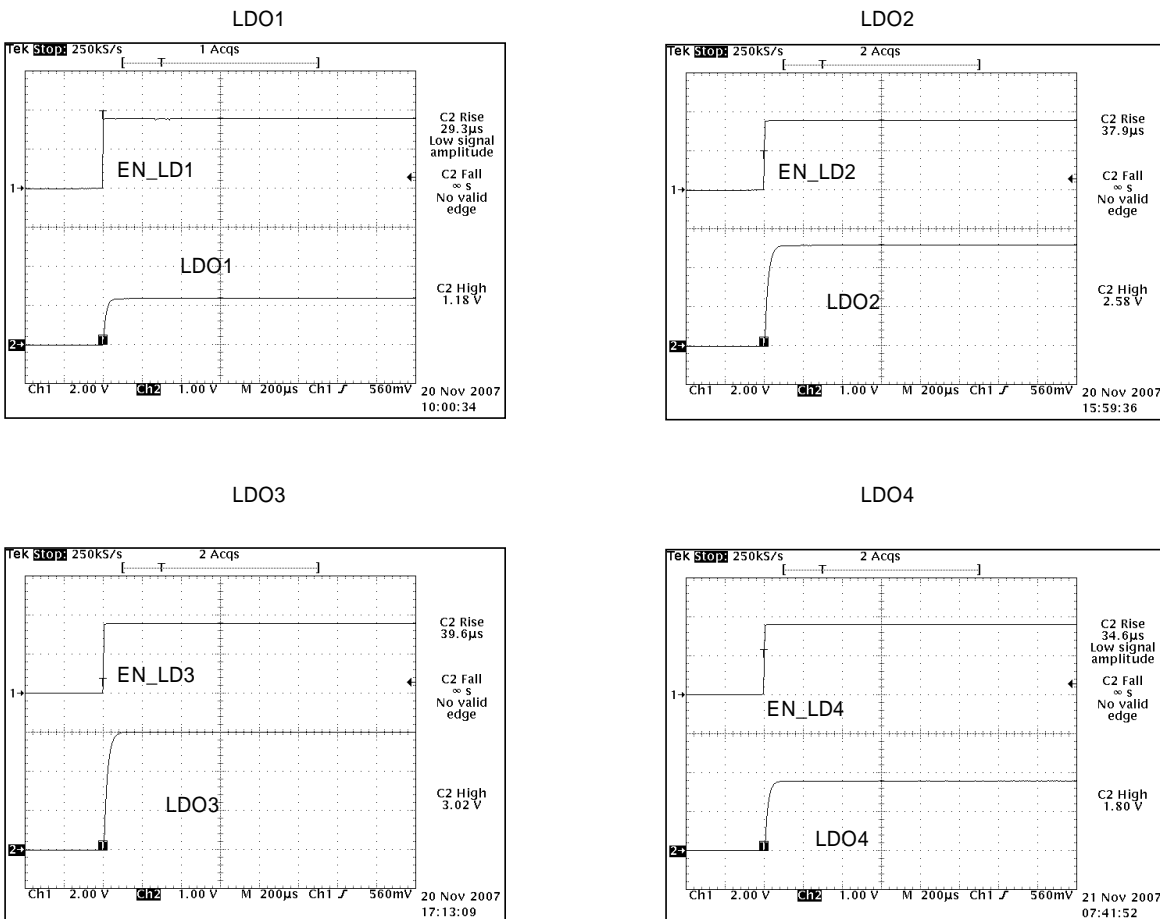
● Reference data(VBAT line transient response)

LDO1

LDO2

LDO3

LDO4

LDO5
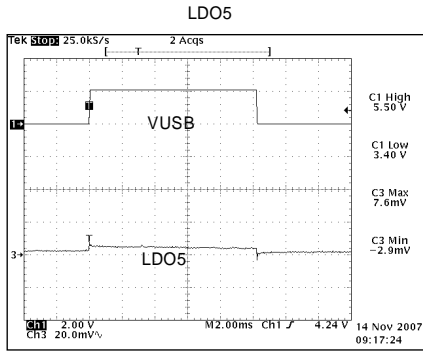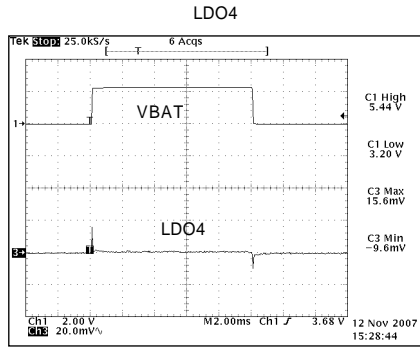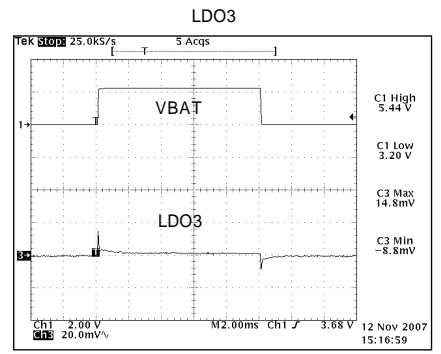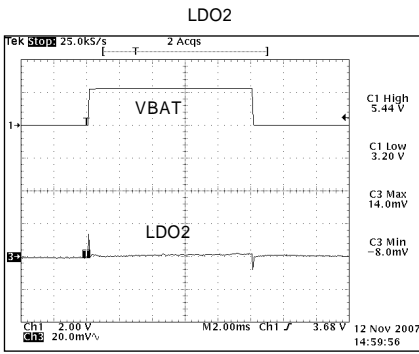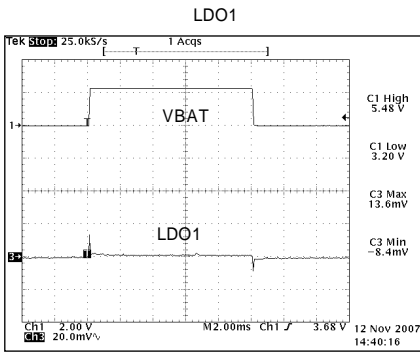
● Use-related Cautions

(1) Absolute maximum ratings
   If applied voltage (VBAT, VADP, VUSB), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range
   This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector
   There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines
   In the design of the board pattern, make power supply and GND line wiring low impedance.
   When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.
   Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(5) GND voltage
   Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation
   When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields
   Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board
   When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins
   Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern
   When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors
   When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal shutdown circuit (TSD)
   When the junction temperature becomes higher than a certain specific value, the thermal shutdown circuit operates and turns the switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.
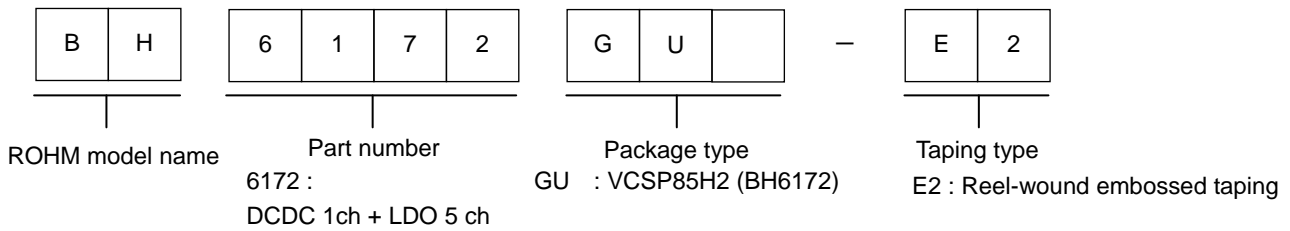
(13) Thermal design
   Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.
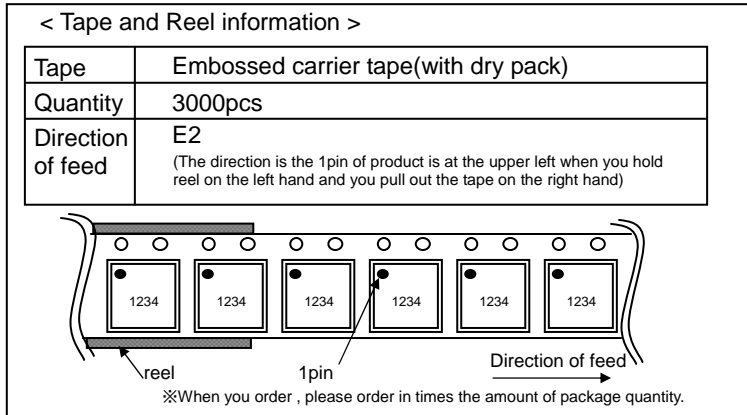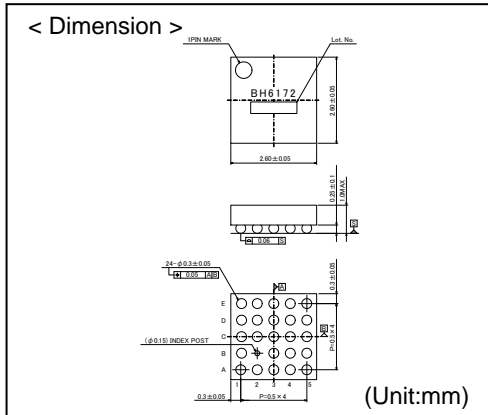
(14) Rush Current
   Extra care must be taken on power coupling, power, ground line impedance, and PCB design while excess amount of rush current might instantly flow through the power line when powering-up a LSI which is equipped with several power supplies, depending on on/off sequence, and ramp delays.

● Selecting a Model Name When Ordering

| B | H | | | 6 | 1 | 7 | 2 | | G | U | | — | E | 2 |

ROHM model name

Part number
6172 :
DCDC 1ch + LDO 5 ch

Package type
GU : VCSP85H2 (BH6172)

Taping type
E2 : Reel-wound embossed taping

VCSP85H2 (BH6172GU)

< Dimension >

IPIN MARK   Lot. No.

BH6172

2.60±0.05
2.80±0.05

0.25±0.1
1.0MAX

0.06

24-φ0.3±0.05
0.05

E
D
C
B
A

(φ0.15) INDEX POST

0.3±0.05
0.3±0.05

1 2 3 4
P=0.5×4

P=0.5×4

(Unit:mm)

< Tape and Reel information >

Tape	Embossed carrier tape(with dry pack)
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

1234 1234 1234 1234 1234 1234

reel   1pin   Direction of feed

※When you order , please order in times the amount of package quantity.

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ROHM

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Published by
KTC LSI Development Headquarters
LSI Business Pomotion Group

Catalog No.08T305A '08.9 ROHM ©

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